In re Patent Application of:
CORONEL ET AL.
Serial No. **10/042,520**
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In the Specification:

Please replace the paragraph beginning at page 8, line 13, with the following rewritten paragraph:

B1

At this stage, an original step of the method according to the present invention includes removing the silicon oxide layer TEOS. This removal is carried out by chemical etching to a thickness of about 4000 Å, and thus ~~create~~ creates a difference in topography between each lower electrode elec 1 and the silicon oxide layer TEOS. The depth removed is defined by the etching time, as illustrated in Figure 6.

Please replace the paragraph beginning at page 8, line 21, with the following rewritten paragraph:

B2

Once this removal is carried out, a dielectric layer dielec, ~~not shown~~ as shown in Figure 6, is deposited. The dielectric chosen is silicon nitride because of its high permittivity. This deposition is preceded by oxidation of the polysilicon. Therefore, the dielectric is formed from two layers, one oxide layer and one nitride layer. The dashed line within the dielectric layer dielec in Figure 6 illustrates these two layers.

Please replace the paragraph beginning at page 9, line 4, with the following rewritten paragraph:

B3

The polysilicon layer elec 2 has a thickness of 1000 Å, and completely fills the cylinders of the capacitances and

the inter-elec 1 space, which has a width D1, ~~D1 on~~ with D1 being on the order of 2000 Å. The inter-elec 1 space of width D2, ~~D2 is~~ with D2 being on the order 7500 Å, which is much wider than D1 and is, therefore, not entirely blocked by the layer of polysilicon elec 2. The difference in topography produced by the removal of silicon oxide TEOS is retained only in zone A, i.e., the zone which must be opened to insert the bit line contact.